REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R032-95. – drw	94-11-08	Michael A. Frye
B	Changes in accordance with NOR 5962-R074-96. – sbr	96-03-08	Michael A. Frye
C	Incorporate rev. A and rev. B NOR's. Update drawing to reflect current requirements. – drw.	02-08-07	Raymond Monnin

REV																				
SHEET																				
REV	C	C	C	C	C	C														
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-01-14

REVISION LEVEL
C

MICROCIRCUIT, LINEAR, 12-BIT, QUAD D/A CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88719**

SHEET 1 OF 21

DSCC FORM 2233
APR 97

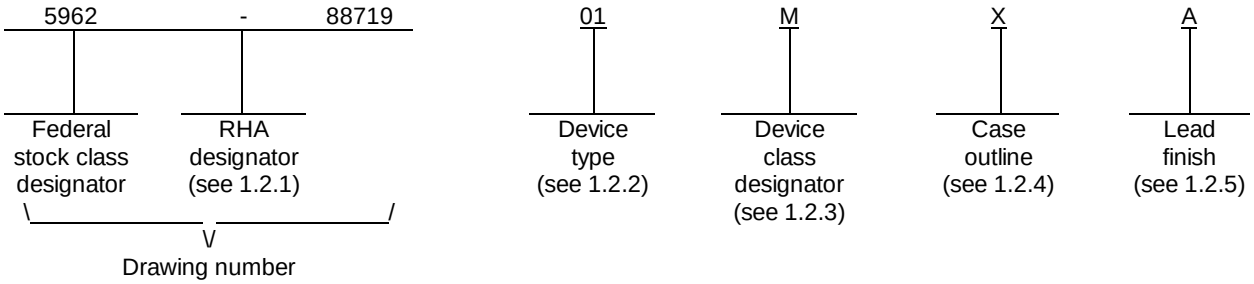
5962-E509-02

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD664TD-UNI	D/A converter, 12-bit, unipolar
02	AD664TD-BIP	D/A converter, 12-bit, bipolar
03	AD664TE	D/A converter, 12-bit, unipolar/bipolar

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in line
Y	CQCC1-N44	44	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{LL} to DGND	0 V dc to +7 V dc
V_{CC} to DGND	0 V dc to +18 V dc
V_{EE} to DGND	-18 V dc to 0 V dc
Power dissipation (P_D)	1000 mW
AGND to DGND	-1 V dc to +1 V dc
Reference input	$V_{REF} \leq \pm 10$ V dc and $V_{REF} \leq (V_{CC} - 2$ V, $V_{EE} + 2$ V)
V_{CC} to V_{EE}	0 V dc to +36 V dc
Digital inputs	-0.3 V dc to +7 V dc
Analog inputs	Indefinite shorts to V_{CC}, V_{LL}, V_{EE} and GND
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Input voltage requirements:	
V_{LL} max	+5.0 V dc
V_{CC}/V_{EE}	±15 V dc
Ambient temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 92 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1, 2, 3	All		12	Bits
Relative accuracy	RA		1	01, 02		±3/4	LSB
				03		±1/2	
			2, 3	01, 02		±1	
				03		±3/4	
			12	01, 02		±1/2	
Differential nonlinearity	DNL	Major carry errors	1	01, 02		±3/4	LSB
				03		±1/2	
			2, 3	All		±1	
			12	01,02		±1/2	
Gain error	A_E	All bits on	1	01, 02		±7	LSB
				03		±5	
			12	01, 02		±5	
Gain temperature coefficient	TCA_E	All bits on	1, 2, 3	All		±10	ppm/°C
Unipolar offset error	V_{OS}	All bits off	1	01		±2	LSB
				03		±1	
			12	01		±1	
Unipolar offset temperature coefficient	TCV_{OS}	All bits off	1, 2, 3	01, 03		±2	ppm/°C
Bipolar zero error 2/	B_{PZE}	MSB on, all others off	1	02		±3	LSB
				03		±2	
			12	02		±2	
Bipolar zero temperature coefficient	TCPZE	MSB 0n, all others off	1, 2, 3	02, 03		±10	ppm/°C
Reference input resistance	R_{IN}	3/	1	All	1.3	2.6	kΩ
Reference voltage range 4/	V_{REF}	3/	1	All	$V_{EE}+2$	$V_{CC}-2$	V
Voltage output, UNI 5/	V_{OU}	3/	1	01, 03	0	$V_{CC}-2$	V
Voltage output, BPI	V_{OB}	3/	1	02, 03	$V_{CC}-2$	$V_{EE}+2$	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output current	I_O	3/	1	All	5		mA
Current, short circuit	I_{SC}	3/	1	All		40	mA
Power supply current	I_{LL}	V_{CC} = +16.5 V, V_{EE} = -16.5 V, V_{IH} = +2.4 V, V_{IL} = +0.4 V	1	All		6	mA
		V_{CC} = +16.5 V, V_{EE} = -16.5 V, $V_{IH} = V_{LL}$, V_{IL} = 0 V				1	
	I_{CC}	I_{CC}: All bits on				15	
	I_{EE}	I_{EE}: All bits on				19	
Gain matching error 6/	mA_E		1	01, 02		±6	LSB
				03		±4	
			12	01, 02		±4	
Bipolar zero matching Error 7/	mB_{PZE}		1	02		±3	LSB
				03		±2	
			12	02		±2	
Offset matching error 8/	mV_{OS}		1	01		±2	LSB
				03		±1	
			12	01		±1	
Digital input high voltage	V_{IH}		1, 2, 3	All	2.0		V
Digital input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Digital inputs high current	I_{IH}	$V_{IN} = V_{LL}$: Data inputs	1, 2, 3	All		±10	µA
		$V_{IN} = V_{LL}$: $\overline{CS}$ /DS0/DS1/ $\overline{RST}$ / $\overline{RD}$ / $\overline{LS}$				±10	
		$V_{IN} = V_{LL}$: $\overline{MS}$ / $\overline{TR}$ 9/			±10		
		$V_{IN} = V_{LL}$: $\overline{QS0}$ / $\overline{QS1}$ / $\overline{QS2}$ 9/				±10	
Digital inputs low current	I_{IL}	V_{IN} = DGND: Data inputs	1, 2, 3	All		±10	µA
		V_{IN} = DGND: $\overline{CS}$ /DS0/DS1/ $\overline{RST}$ / $\overline{RD}$ / $\overline{LS}$				±10	
		V_{IN} = DGND: $\overline{MS}$ / $\overline{TR}$ 9/				-10	
		V_{IN} = DGND: $\overline{QS0}$ / $\overline{QS1}$ / $\overline{QS2}$ 9/				±10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital out low voltage	V_{OL}		1, 2, 3	All		+0.4	V
Digital out high voltage	V_{OH}		1, 2, 3	All	+2.4		V
Power supply gain sensitivity	PSGS	$11.4 V \le V_{CC} \le 16.5 V$	1	All	±5		ppm/%
		$-16.5 V \le V_{EE} \le -11.4 V$					
		$4.5 V \le V_{LL} \le 5.5 V$					
$\overline{CS}$ pulse width	t_{CW}	Data input mode 10/ (figure 4 diagram A and B)	9	All	80		ns
			10, 11		100		
Data setup	t_{DS}	Data input mode 10/ (figure 4 diagram A)	9, 10, 11	All	0		ns
Data hold	t_{DH}		9, 10, 11		15		
Address setup	t_{AS}		9, 10, 11		0		
Address hold	t_{AH}		9, 10, 11		15		
$\overline{LS}$ setup	t_{LS}		9, 10, 11		0		
$\overline{LS}$ hold	t_{LH}		9, 10, 11		15		
Data setup	t_{DS}	Data input mode 10/ (figure 4 diagram C)	9, 10, 11	All	0		ns
Data hold	t_{DH}		9, 10, 11		0		
$\overline{LS}$ width	t_{LW}		9		60		
			10, 11		80		
$\overline{LS}$ setup	t_{LS} 11/		9, 10, 11		0		
$\overline{CS}$ hold	t_{CH}		9		30		
			10, 11		50		
Address setup	t_{AS}		9, 10, 11		0		
Address hold	t_{AH}		9, 10, 11		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{MS}$ setup	t_{MS}	Mode select 10/ (figure 4 diagram D)	9, 10, 11	All	0		ns
Address setup	t_{LS} 11/		9, 10, 11		0		
Data setup	t_{DS}		9, 10, 11		0		
$\overline{LS}$ width	t_{LW}		9		60		
			10, 11		70		
$\overline{CS}$ hold	t_{CH}		9		70		
			10, 11		80		
Data hold	t_{DH}		9, 10, 11		0		
$\overline{MS}$ hold	t_{MH}		9, 10, 11		0		
Mode select	t_{MS}	Mode select 10/ (figure 4 diagram E)	9, 10, 11	All	0		ns
$\overline{MS}$ hold	t_{MH}		9, 10, 11		15		
$\overline{LS}$ setup	t_{LS} 11/		9, 10, 11		0		
Data setup	t_{DS}		9, 10, 11		0		
$\overline{CS}$ width	t_W		9		80		
			10, 11		100		
$\overline{LS}$ hold	t_{LH}		9, 10, 11		15		
Data hold	t_{DH}		9, 10, 11		15		
Reset width		Asynchronous mode 10/ (figure 4 diagram F)	9 10, 11		80 100		ns
Functional tests	FT	See paragraph 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address setup	t_{AS}	Readback mode 10/ (figure 4 diagram G and H)	9, 10, 11	All	0		ns
Address hold	t_{AH}		9, 10, 11		0		
$\overline{RD}$ setup	t_{RS}		9, 10, 11		0		
$\overline{RD}$ hold	t_{RH}		9, 10, 11		0		
$\overline{MS}$ setup	t_{MS}		9, 10, 11		0		
$\overline{MS}$ hold	t_{MH}		9, 10, 11		0		
Data access	t_{DV}		9		150		
			10, 11		180		
Data release	t_{DF}		9		60		
			10, 11		75		
Address setup	t_{AS}	Transparent mode 10/ (figure 4 diagram I)	9, 10, 11	03	0		ns
Quad select setup	t_{QS}		9, 10, 11		0		
Transparent setup	t_{TS}		9, 10, 11		0		
Transparent width	t_{TW}		9		80		
			10, 11		90		
Chip select hold	t_{CH}		9		90		
			10, 11		110		
Data hold	t_{DH}		9, 10, 11		0		

1/ V_{CC} = +15 V, V_{EE} = -15 V, 50Ω resistor pin 6 to pin 7, A0, A1, A2, A3, $\overline{CS}$ = logic "0", V_{IH} = 2.0 V, V_{IL} = 0.8 V, unipolar configuration.
2/ Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.
3/ Parameter is guaranteed by design, not tested.
4/ A minimum power supply of ±12.0 V is required for a 10 V reference voltage.
5/ A minimum power supply of ±12.0 V is required for 0 to +10 V and ±10 V operation. A minimum power supply of ±11.4 V is required for –5 V to +5 V operation.
6/ Gain error matching is the largest difference in gain error between any two DACs in one package.
7/ Bipolar zero matching is the largest difference in bipolar zero error between any two DACs in one package.
8/ Offset error matching is the largest difference in offset error between any two DACs in one package.
9/ Device type 03 only.
10/ Timing specifications are relative to $\overline{CS}$, V_{CC} = +15 V, V_{EE} = -15 V, V_{REF} = +10 V, V_{IH} = 2.4 V, V_{IL} = 0.4 V. Specifications are guaranteed but not tested. Refer to figure 4.
11/ For $t_{LS} > 0$, the width of $\overline{LS}$ must be increased by the same amount that t_{LS} is greater than 0 ns.

Device types	01 and 02	03
Case outlines	X	Y
Terminal number	Terminal symbol	
1	V_{REF}	$\overline{RD}$
2	$V_{OUT}C$	$\overline{LS}$
3	$V_{OUT}D$	NC
4	$\overline{CS}$	AGND
5	DS0	V_{CC}
6	DS1	V_{EE}
7	DGND	R_FA
8	$\overline{RST}$	$V_{OUT}A$
9	DB0(LSB)	$V_{OUT}B$
10	DB1	R_FB
11	DB2	V_{REF}
12	DB3	R_FC
13	DB4	$V_{OUT}C$
14	DB5	$V_{OUT}D$
15	DB6	R_FD
16	DB7	NC
17	DB8	NC
18	DB9	$\overline{CS}$
19	DB10	DS0
20	DB11(MSB)	DS1
21	V_{LL}	DGND
22	$\overline{RD}$	$\overline{RST}$
23	$\overline{LS}$	$\overline{QS0}$
24	AGND	$\overline{QS1}$
25	V_{CC}	$\overline{QS2}$
26	V_{EE}	$\overline{TR}$
27	$V_{OUT}A$	$\overline{MS}$
28	$V_{OUT}B$	DB0(LSB)
29	---	DB1
30	---	DB2
31	---	DB3
32	---	DB4
33	---	DB5
34	---	NC
35	---	DB6
36	---	DB7
37	---	DB8
38	---	DB9
39	---	DB10
40	---	DB11(MSB)
41	---	NC
42	---	V_{LL}
43	---	NC
44	---	NC

FIGURE 1. Terminal connections.

Function	DS1, DS0	$\overline{LS}$	$\overline{MS}$	$\overline{TR}$	$\overline{QS0}$, $\overline{1}$, $\overline{2}$ (see note 1)	$\overline{RD}$	$\overline{CS}$	$\overline{RST}$
Load 1st rank								
DAC A	00	0	1	1	Select quad	1	1→0	1
DAC B	01	0	1	1	Select quad	1	1→0	1
DAC C	10	0	1	1	Select quad	1	1→0	1
DAC D	11	0	1	1	Select quad	1	1→0	1
Load 2nd rank	XX	1	1	1	XXX	1	1→0	1
Read 2nd rank	Select D/A	X	1	1	Select quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
Transparent (see note 1)								
All DACs	XX	1	1	0	000	1	1→0	1
DAC A	00	0	1	0	000	1	1→0	1
DAC B	01	0	1	0	000	1	1→0	1
DAC C	10	0	1	0	000	1	1→0	1
DAC D	11	0	1	0	000	1	1→0	1
Mode select (see notes 1 and 2)								
1st rank	XX	0	0	1	00X	1	1→0	1
2nd rank	XX	1	0	1	XXX	1	1→0	1
Readback mode (see note 1)	XX	X	0	1	00X	0	1→0	1

NOTES:
1. For device type 03 only.
2. For $\overline{MS}$, $\overline{TR}$, $\overline{LS}$ = 0, a $\overline{MS}$ 1st write occurs.
3. X = Don't care.

FIGURE 2. Truth table.

28-Terminal

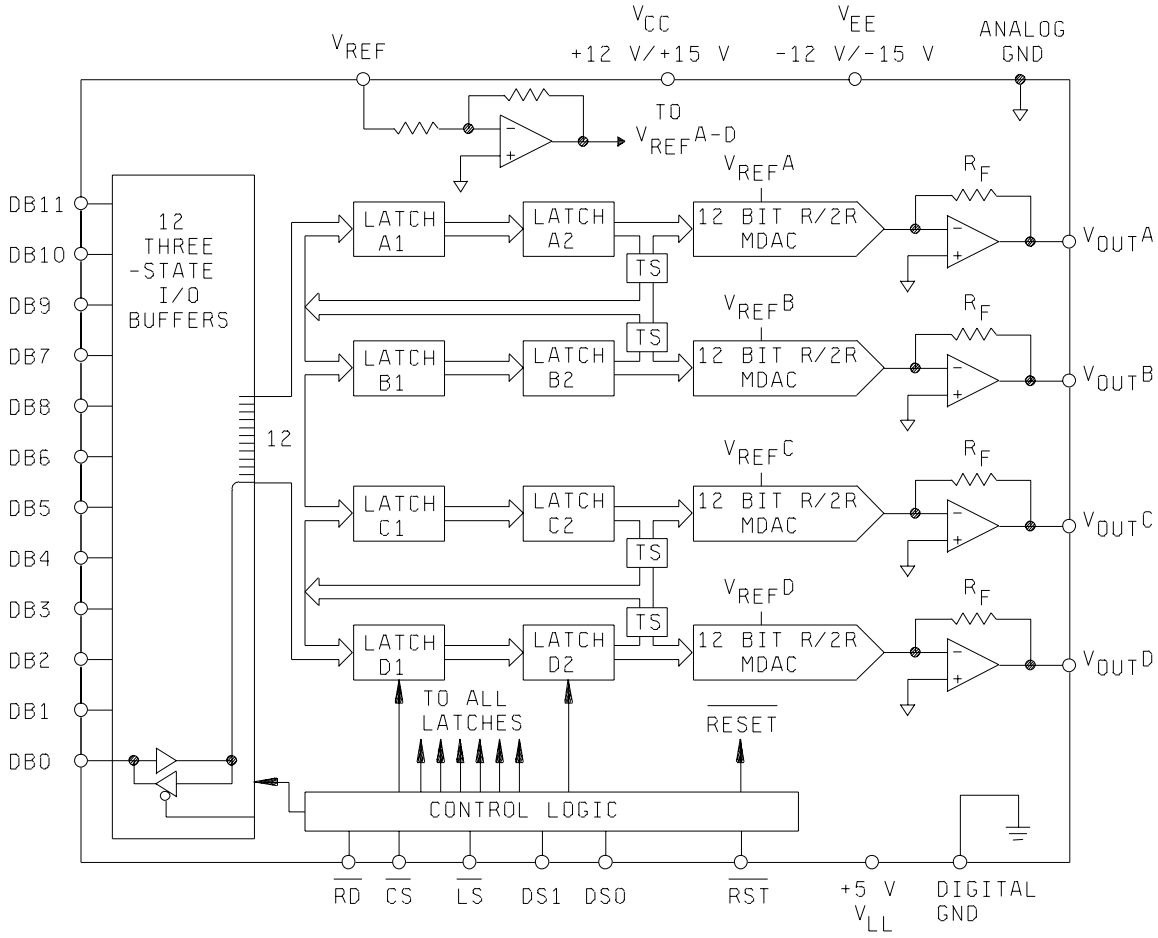


FIGURE 3. Block diagram.

44-Terminal

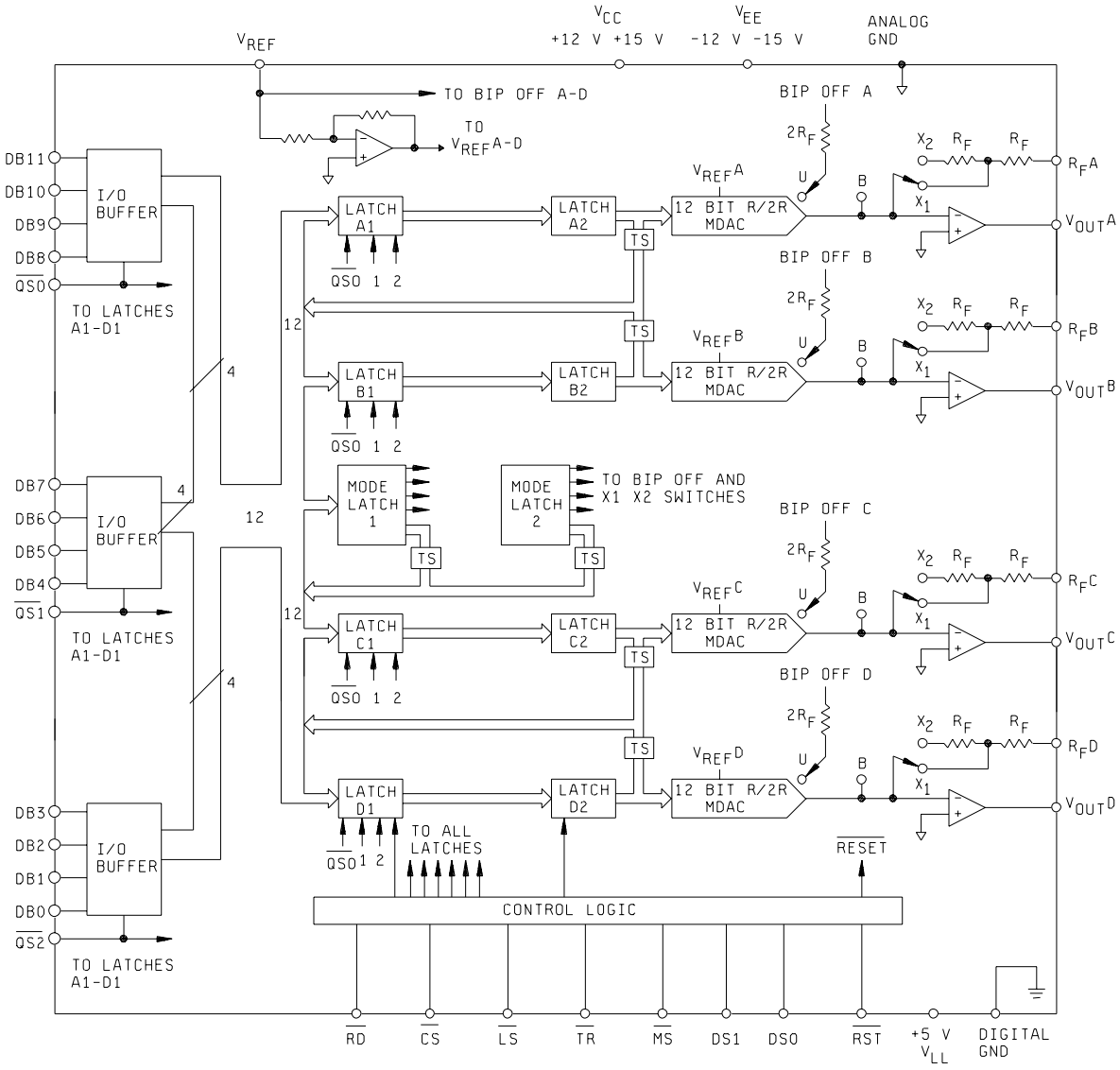


FIGURE 3. Block diagram - continued.

Preload first rank of DAC

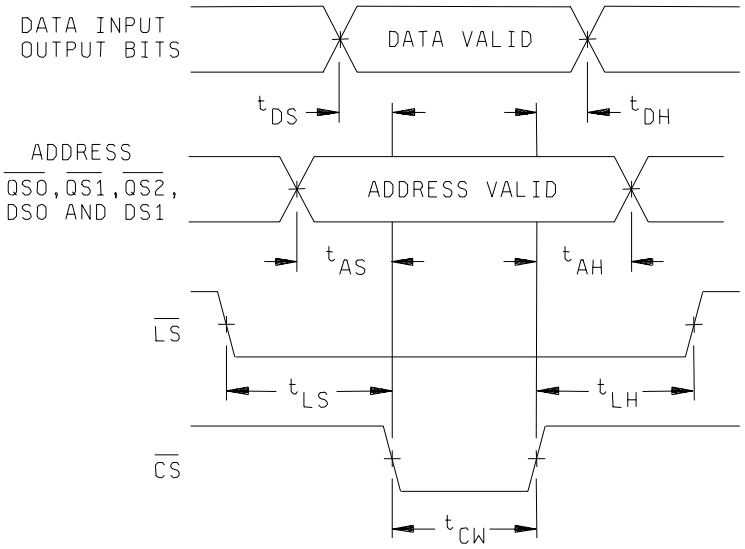


Diagram A

Update second rank of a DAC

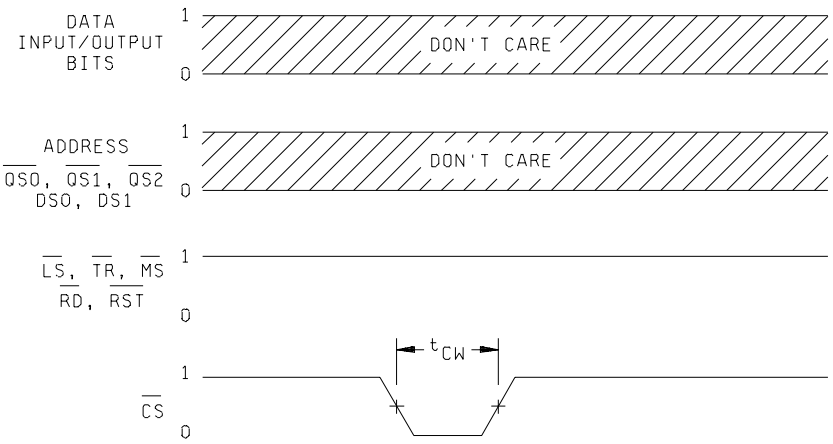


Diagram B

FIGURE 4. Timing diagram.

Update output of a single DAC

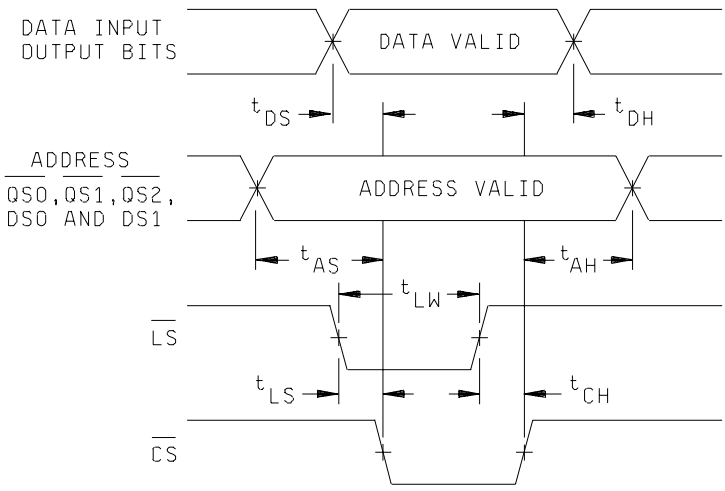


Diagram C

Load and update mode of one DAC

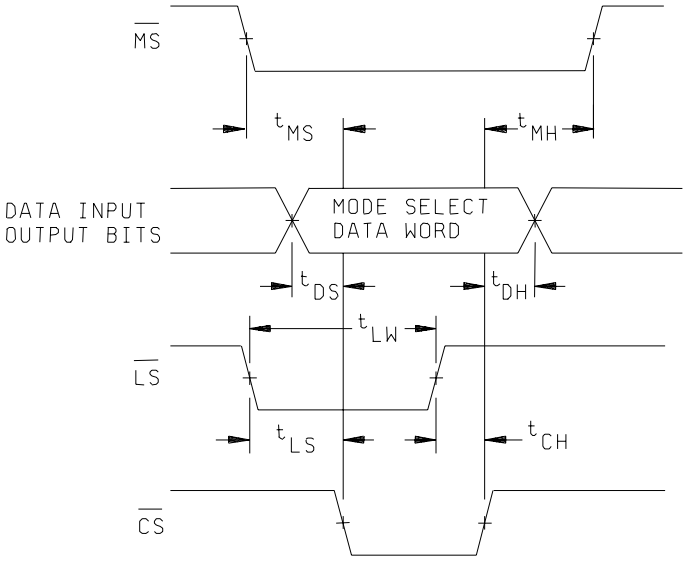


Diagram D

FIGURE 4. Timing diagram - continued.

Preload mode select register

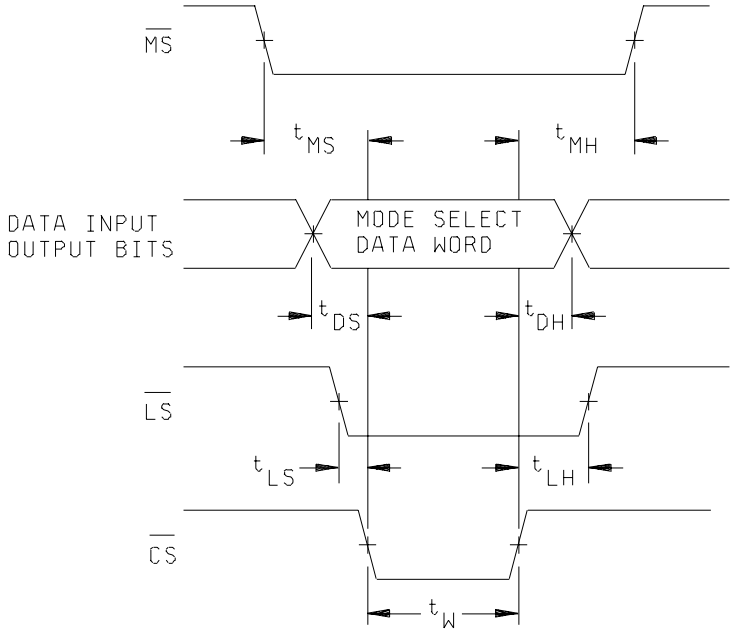


Diagram E

Asynchronous reset operation

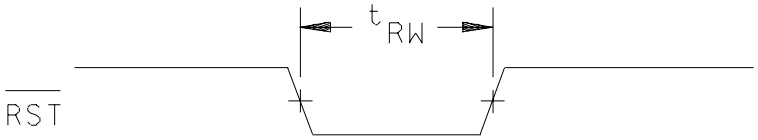


Diagram F

FIGURE 4. Timing diagram - continued.

DAC input code readback

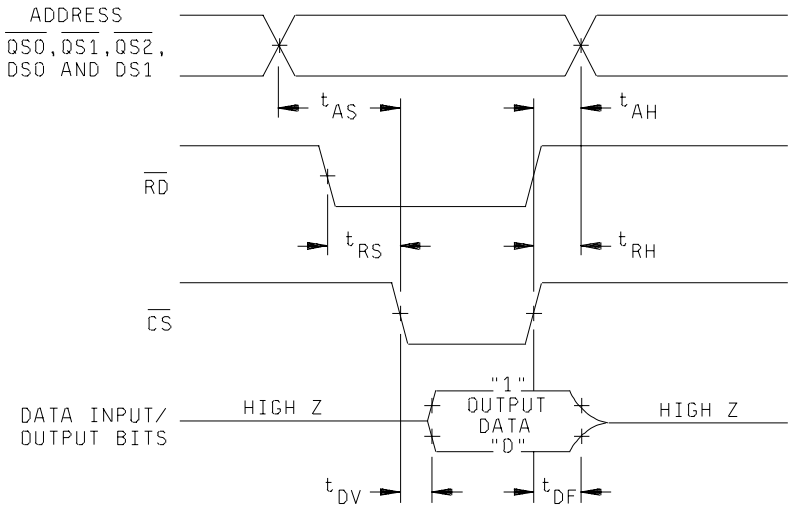


Diagram G

Mode select readback

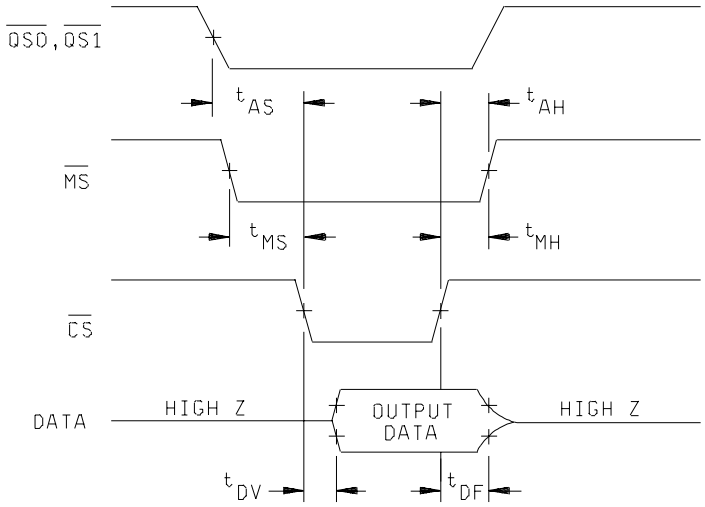


Diagram H

FIGURE 4. Timing diagram - continued.

Fully Transparent mode

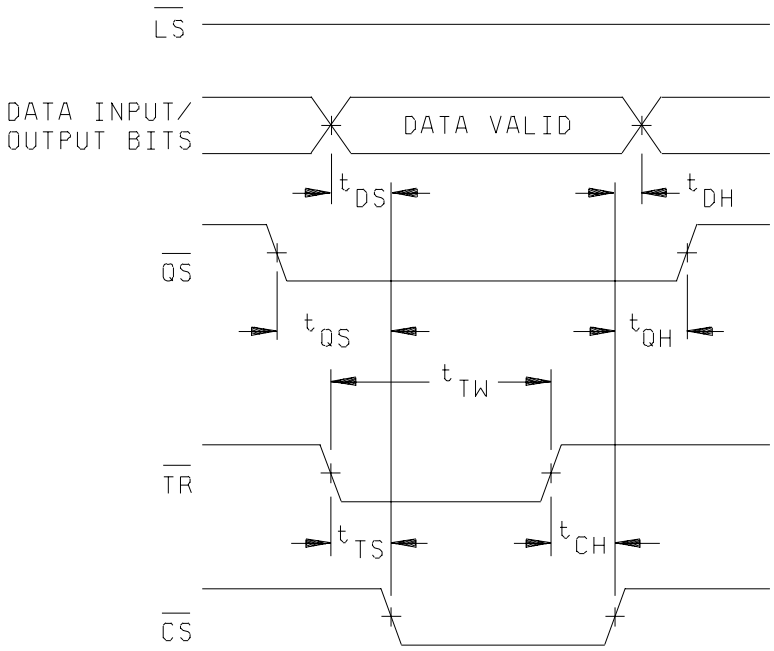


Diagram I

FIGURE 4. Timing diagram - continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Special subgroup 12 (as referenced in table I) added for grading and selection tests at +25°C.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 9, 10, 11	1/ 1, 2, 3, 9, 10, 11	1/ 1, 2, 3, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1	1, 2, 3, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-08-07

Approved sources of supply for SMD 5962-88719 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8871901MXA	24355	AD664TD-UNI/883B
5962-8871902MXA	24355	AD664TD-BIP/883B
5962-8871903MYA	24355	AD664TE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462